

AREA EFFICIENT STACKING OF ANTIFUSES

IN SEMICONDUCTOR DEVICE

Abstract of the Disclosure

A semiconductor device is provided which is formed of a  
5 wafer having on a surface thereof an area efficient arrangement  
of at least two antifuses in vertically stacked relation and  
sharing a common intermediate electrode therebetween. The  
arrangement includes at least one lower antifuse having a lower  
counter electrode and a lower fusible insulator portion defining  
10 a lower fuse element of an initial high electrical resistance  
state which interconnects the lower counter electrode with the  
common intermediate electrode, and at least one upper antifuse,  
which may be the same as or different from the lower antifuse,  
the upper antifuse having an upper counter electrode and an upper  
45 fusible insulator portion defining an upper fuse element of an  
initial high electrical resistance state which interconnects the  
upper counter electrode with the common intermediate electrode.